AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently amended) A keeper circuit for a dynamic node of a circuit, wherein the effective strength of the keeper circuit operating on the dynamic node is reduced from a first non-zero strength level to a second non-zero strength level during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device and wherein the effective strength of the keeper circuit operating on the dynamic node is restored to the first non-zero strength level after arrival of a latest signal transitioning to a level that can discharge the dynamic node.

2. (Original) The circuit, as recited in claim 1, wherein the sensitivity of the at least one path includes output of an incorrect value of the evaluation circuit output.

3. (Original) The circuit, as recited in claim 1, wherein a response to the sensitivity is otherwise a reduced speed of the evaluation circuit output.

4. (Cancelled)

5. (Currently amended) A circuit comprising:

a dynamic node;

an evaluation circuit coupled to the dynamic node; ~~and~~

a keeper circuit coupled to the dynamic node, wherein the keeper circuit has a first non-zero strength during a first interval and a second non-zero strength during a second interval, the first non-zero strength being substantially greater than the second non-zero strength; and

wherein the first interval begins before arrival of an earliest signal transitioning to a level that can discharge the dynamic node; and

wherein the second interval begins after arrival of a latest signal transitioning to a level that can discharge the dynamic node.

6. (Original) The circuit, as recited in claim 5, wherein the keeper circuit latches an output of the circuit.

7. (Previously presented) The circuit, as recited in claim 5, wherein the keeper circuit includes a first keeper device.

8. (Previously presented) The circuit, as recited in claim 7, wherein the keeper circuit includes a keeper gating device coupled to the first keeper device and the dynamic node.

9. (Previously presented) The circuit, as recited in claim 5, wherein the keeper circuit includes a weak keeper device coupled to the dynamic node.

10. (Original) The circuit, as recited in claim 5, wherein the keeper circuit is responsive to a keeper control.

11. (Original) The circuit, as recited in claim 10, wherein the keeper control is clocked.

12. (Original) The circuit, as recited in claim 10, wherein the keeper control is self-timed.

13. (Previously presented) The circuit, as recited in claim 5, further comprising:
a clock node;
a precharge device coupled to the clock node and the dynamic node; and
a discharge device coupled to the clock node and the evaluation circuit.

14. (Original) The circuit, as recited in claim 13, wherein the precharge device and the evaluation circuit operate during different phases of a control signal.

15. (Previously presented) The circuit, as recited in claim 7, wherein the first keeper device is sized to sufficiently overcome the leakage current in the evaluation circuit.

16. (Previously presented) The circuit, as recited in claim 5, wherein a reduction in the effective strength of the keeper circuit from the first non-zero strength to the second non-zero strength occurs before arrival of an earliest signal transitioning to a level that can discharge the dynamic node.

17. (Previously presented) The circuit, as recited in claim 5, wherein the effective keeper circuit strength is restored to the first non-zero strength from the second non-zero strength after arrival of a latest signal transitioning to a level that can discharge the dynamic node.

18. (Previously presented) The circuit, as recited in claim 9, wherein the weak keeper device is minimally sized to sufficiently overcome noise while a first keeper device is effectively disabled.

19. (Original) The circuit, as recited in claim 5, wherein the dynamic node is precharged high.

20. (Original) The circuit, as recited in claim 19, wherein the evaluation circuit is n-logic.

21. (Original) The circuit, as recited in claim 5, wherein the dynamic node is precharged low.

22. (Original) The circuit, as recited in claim 21, wherein the evaluation circuit is p-logic.

23. (Currently amended) A method for evaluating a dynamic node, comprising:
precharging a dynamic node;
effectively disabling a first keeper device coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device;
evaluating an evaluation circuit;
protecting the dynamic node from noise during the interval; and

effectively enabling the first keeper device after arrival of a latest signal transitioning to a level that can discharge the dynamic node.

24. (Cancelled)

25. (Currently amended) A method for weakening a keeper circuit, comprising:

reducing effective keeper circuit strength from a first non-zero strength to a second non-zero strength during an interval in which at least one path of an evaluation circuit is sensitive to a keeper device; and

restoring the effective keeper circuit strength to the first non-zero strength after arrival of a latest signal transitioning to a level that can discharge an associated dynamic node.

26. (Original) The method, as recited in claim 25 for weakening a keeper circuit, further comprising:

maintaining a weak keeper device during the interval.

27. (Currently amended) An apparatus for evaluating a dynamic node, comprising:

a dynamic node;

a first keeper device coupled to the dynamic node;

means for precharging the dynamic node;

means for effectively disabling the first keeper device coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device;

means for protecting the dynamic node from noise during the interval;

means for evaluating an evaluation circuit; and

means for effectively enabling the first keeper device after arrival of a latest signal transitioning to a level that can discharge the dynamic node.

28. (Cancelled)

29. (Cancelled)

30. (Previously presented) A circuit comprising:

a dynamic node;

a precharge device coupled to the dynamic node;

an evaluation circuit coupled to the dynamic node;

a discharge device coupled to the evaluation circuit;

a clock node coupled to the precharge device and the discharge device;

a keeper circuit coupled to the dynamic node, wherein a first keeper device is selectively disabled during a first interval;

at least a second keeper device, the second keeper device being coupled to the dynamic node;

wherein a gain of the first keeper device is substantially greater than a gain of the second keeper device.

31. (Previously presented) The circuit, as recited in claim 30, wherein the evaluation circuit overcomes the second keeper.

32. (Previously presented) The circuit, as recited in claim 30, wherein the second keeper has a gain sufficient to overcome noise but insufficient to overcome leakage current in the evaluation circuit.

33. (Previously presented) The circuit, as recited in claim 30, further comprising:

a keeper gating device coupling the first keeper device to the dynamic node.

34. (Previously presented) The circuit, as recited in claim 30, wherein the first keeper has a gain sufficient to overcome leakage current in the evaluation circuit.

35. (Previously presented) The circuit, as recited in claim 23, wherein the dynamic node is protected by at least a weak keeper.

36. (Previously presented) The circuit, as recited in claim 27, wherein the means for protecting the dynamic node comprises a weak keeper.